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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/981,734	10/19/2001	Tsuyoshi Tamura	110927	6121

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	PAPER NUMBER
3663	

DATE MAILED: 03/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/981,734	TAMURA ET AL.	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 12/20/05 forms the basis for this office action. In said Amendment applicant substantially amended all pending claims 22-24.

Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claims 22-24*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Vainsenscher (5,977,997) (previously made of record) in view of Oguro et al (6,301,430 B1) (previously made of record), Ouyang et al (6,614,442 B1) and Ilcisin et al (5,978,052), or, in the alternative, in view of Oguro et al, Ouyang et al and Mangerson et al (5,914,711).

Vainsencher teaches a semiconductor device (col. 4, l. 30-48) for driving a display section (col. 4, l. 5-25), the semiconductor device comprising:

a first input terminal to which compressed data is input (stream i/o interface 230 (col. 5, l. 32-44);

a decoder 206 (col. 4, l. 54-65) which decompresses the compressed data;

a RAM 218 (col. 5, l. 15-31) which stores a decode data by the decoder; a driving section 240 (col. 5, l. 45-64) which is connected to an electrode of the display section; and a controller 202 (col. 6, l. 41) which controls the decoder, the RAM and the driving section. The newly added limitation that said controller not only (in general terms) controls the decoder, the RAM and the driving section, but actually controls the *timing* of decoder, RAM and driving section *does not further limit* the device because an MPEG as taught by Vainsenscher (abstract, e.g.) inherently has a controller which controls decode timing of said decoder and a RAM such as 218 in Vainsenscher inherently has a controller to read the timing of said reading, the controller of driving section being inherently one of time control.

Vainsencher does not necessarily specifically teach the limitations

(A) "wherein a write speed of the decoded data for one frame into the RAM is higher than the read speed of the display data for one frame of the RAM", nor

(B) of first and second frame buffers each storing the decoded data for one frame by the decoder and that the decoded data stored by the RAM are read out from said first and second frame buffers and

(C) the controller causes decoded data to be written into the frame buffer from which decoded data is <u>not</u> output to the RAM .

However, ad (A) it would have been obvious to include said limitation (A) in view of Oguro et al, who, in a patent on inter alia a device for driving a display section ("Reproducing Circuit" driving a video display; see cols. 21-22), hence analogous art, teach the write speed of the decoded data for one frame into a memory for temporary

memory storage (FIFO analogous to the RAM) to be higher than the read speed of the display data for one frame from said temporary memory storage (col. 22, l. 6-10), so as to ensure there is always data present in the memory and an underflow condition is avoided (col. 22, l. 6-10). *Motivation* to include the teaching by Oguro et al in the invention by Vainsencher thus immediately is seen to flow from the undesirability of trying to read when nothing is written in the first place, also in the device by Vainsencher et al.

Furthermore, ad (B) it would have been obvious to include said limitation (B) in view of Ouyang et al, who teach that "frame buffers are usually used by an MPEG compliant decoding process to store decoded I-picture and/or P-picture until all pictures depending on the I-picture and/or P-picture for motion compensation are reconstructed" (see col. 2, l. 65 – col. 3, l. 7). Said limitation (B) is thus seen to only reflect conventional practice for the purpose of ensuring chronology necessary for proper chronology in the process of reconstruction.

Motivation to include the limitation (B) as taught by Ouyang et al thus immediately follows from the need to ensure proper reconstruction.

Finally, ad (C) it has long been conventional art to use at least two, or two functionally different sets of, frame buffers, one for reading directly from the decoder and one for writing, having received the data at a later stage, as witnessed, for instance, by Ilcisin et al (see col. 5, l. 8-12), or by Mangerson et al, teaching different frame buffers (first buffer 401 for the initial reading, buffers 401 and 403 for writing) for read and write operations (col. 8, l. 58 – col. 9, l. 14).

Motivation is implicit in the same teaching of Ilcisin et al and Mangerson et al, i.e., to avoid tearing, which is the known conflict between read and write operations involving frame buffers.

On claim 23: Vainsencher et al do not necessarily specifically discuss a second input terminal for text data. However, Vainsencher et al teach the input and displaying of graphical data. Vainsencher et al further teach their single chip computer system to be for use in video game consoles, DVD players and set-top boxes (see abstract). Examiner takes official notice that graphical data in these environments typically include text data. Therefore, it would have been obvious to one of ordinary skills in the art at the time the invention was made to include an input for text data so that the system could function as a typical game console, DVD play or set-top box.

On claim 24: Vainsencher teaches a semiconductor device (col. 4, l. 30-48) for driving a display section (col. 4, l. 5-25), the semiconductor device comprising: an input terminal to which compressed data is input (stream i/o interface 230 (col. 5, l. 32-44); a decoder 206 (col. 4, l. 54-65) which decompresses the compressed data; a RAM 218 (col. 5, l. 15-31) which stores a decode data by the decoder; a driver 240 (col. 5, l. 45-64) which is connected to an electrode of the display section; and a controller 202 (col. 6, l. 41) which controls the decoder, the RAM and the driver, while, with regard to the limitation "wherein the same decoded data is read out from the RAM at least two times, which the decoded data is decoded for one frame and written into the RAM", said limitation is met as an inherent feature of the MPEG 206 coprocessor: in any MPEG decompression system it is necessary to store and read multiple times the I frames, the

I frame data being required for decompression of the P and B frames. The newly added limitation that said controller not only (in general terms) controls the decoder, the RAM and the driving section, but actually controls the *timing* of decoder, RAM and driving section *does not further limit* the device because an MPEG as taught by Vainsenscher (abstract, e.g.) inherently has a controller which controls decode timing of said decoder and a RAM such as 218 in Vainsenscher inherently has a controller to read the timing of said reading, the controller of driving section being inherently one of time control.

Vainsencher does not necessarily specifically teach the limitations

(A) "wherein a write speed of the decoded data for one frame into the RAM is higher than the read speed of the display data for one frame of the RAM", nor

(B) of first and second frame buffers each storing the decoded data for one frame by the decoder and that the decoded data stored by the RAM are read out from said first and second frame buffers and

(C) the controller causes decoded data to be written into the frame buffer from which decoded data is not output to the RAM .

However, ad (A) it would have been obvious to include said limitation (A) in view of Oguro et al, who, in a patent on inter alia a device for driving a display section ("Reproducing Circuit" driving a video display; see cols. 21-22), hence analogous art, teach the write speed of the decoded data for one frame into a memory for temporary memory storage (FIFO analogous to the RAM) to be higher than the read speed of the display data for one frame from said temporary memory storage (col. 22, l. 6-10), so as to ensure there is always data present in the memory and an underflow condition is

avoided (col. 22, l. 6-10). *Motivation* to include the teaching by Oguro et al in the invention by Vainsencher thus immediately is seen to flow from the undesirability of trying to read when nothing is written in the first place, also in the device by Vainsencher et al.

Furthermore, ad (B) it would have been obvious to include said limitation (B) in view of Ouyang et al, who teach that "frame buffers are usually used by an MPEG compliant decoding process to store decoded I-picture and/or P-picture until all pictures depending on the I-picture and/or P-picture for motion compensation are reconstructed" (see col. 2, l. 65 – col. 3, l. 7). Said limitation (B) is thus seen to only reflect conventional practice for the purpose of ensuring chronology necessary for proper chronology in the process of reconstruction.

Motivation to include the limitation (B) as taught by Ouyang et al thus immediately follows from the need to ensure proper reconstruction.

Finally, ad (C) it has long been conventional art to use at least two, or two functionally different sets of, frame buffers, one for reading directly from the decoder and one for writing, having received the data at a later stage, as witnessed, for instance, by Ilcisin et al (see col. 5, l. 8-12), or by Mangerson et al, teaching different frame buffers (first buffer 401 for the initial reading, buffers 401 and 403 for writing) for read and write operations (col. 8, l. 58 – col. 9, l. 14).

Motivation is implicit in the same teaching of Ilcisin et al and Mangerson et al, i.e., to avoid tearing, which is the known conflict between read and write operations involving frame buffers.

Response to Arguments

Applicant's arguments filed 12/20/2005 have been fully considered but they are not persuasive. The newly added limitations included now for the first time in both independent claims 22 and 24 are seen to be obvious at least over Ouyang et al, in combination with either Ilcisin et al or Mangerson et al, as explained overleaf.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
February 26, 2006

JACK KEITH
SUPERVISORY PATENT EXAMINER